

Flip Chip FBGA (fcCSP)

fcLFBGA, fcTFBGA, fcVFBGA, fcLGA, fcTFBGA-SD2, fcTFBGA-SD3 & fcLFBGA-H

HIGHLIGHTS

- Ultra low interconnect parasitics eliminates wire inductance and resistance compared to wirebond interconnect
- Ultimate miniaturization eliminates wire loops and wire spans compared to conventional wirebond packages
- Ideal package type for RF, Power/Analog and Logic devices for wireless and portable products
- One piece heat spreader can be added for exceptional thermal performance

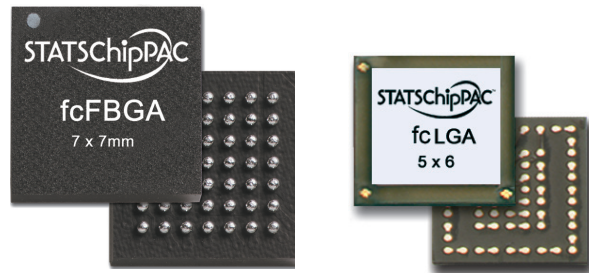
FEATURES

- Eutectic SnPb, hi-Pb or Pb-free bumps, Cu column
- Minimum overall height of 1.40mm for fcLFBGA; 1.20mm for fcTFBGA; 1.00mm for fcVFBGA; 0.65mm for fcLGA
- Conventional 2 and 6 layer through-hole or PPG build-up laminate substrates available
- ABF build-up substrates available
- 150µm minimum die solder bump pitch in production
- 0.40mm min. package ball (BGA) or pad (LGA) pitch in production
- Body sizes 4 x 4mm through 17 x 17mm using matrix strip format
- In-house wafer bumping with plated and printed bumps for 6, 8 & 12 inch wafers including BCB and polyimide re-passivation and RDL option
- Molded underfill (MUF) with solder bump in production; MUF with Cu column bump qualified
- fcLFBGA-H (1-piece heat spreader) with capillary underfill (CUF) qualified
- High density wide strip available

PACKAGE CONFIGURATIONS

Package	Body Size (mm)	Lead Count	Qualified
fcLGA	5 x 6	71	yes
fcLFBGA	7 x 7	49	yes
	13 x 13	144, 504	yes
	14 x 14	976	yes
	15 x 15	603, 1056, 1112	yes
fcLFBGA-H	12 x 12	196	yes
	5 x 7	136	yes
	6 x 6	105	yes
	7 x 7	191	yes
	7.65 x 9.25	170	yes
	10 x 10	384	yes
	11 x 11	456	yes
	12 x 12	424, 452	yes
	15 x 15	782	yes
	17 x 17	400	yes
fcTFBGA-SDx	10 x 10	297	yes
	12 x 12	424	yes
fcVFBGA	6.2 x 7.8	196	yes
	6.2 x 12.6	308	yes
	7 x 5	136	yes
	7 x 7	191	yes
	7.5 x 7.5	221	yes
	11 x 11	344	yes
	12.9 x 9.8	486	yes
	12 x 12	424	yes
	12.6 x 12.6	669	yes
fcFBGA-SIP	7.55 x 10.6	329	yes

Notes: Shown above are qualified packages. Because flip chip packages are custom packages and share mold and singulation tooling with corresponding wirebond packages, there is considerable flexibility in producing a wide range of body sizes with minimal additional tooling.



DESCRIPTION

STATS ChipPAC's fcLFBGA and fcLGA packages form a subgroup in the Flip Chip package family which represents the form factor popularly known in the industry as CSP (Chip Scale Package). The fcLFBGA, fcTFBGA-SD2, fcTFBGA-SD3 and fcLGA are produced on substrates with matrix strip format and use overmolding and saw singulation processes similar to wirebond packages of the same form factors. The fcLFBGA is an overmolded package with solder balls, and fcTFBGA-SD2 and fcTFBGA-SD3 are overmolded hybrid products (flip chip on the bottom and wirebond die on the top), while the fcLGA is an exposed die product that does not have solder balls. The fcLFBGA-H is a high performance thermal package also produced on substrates in matrix strip format; the die is underfilled by capillary underfill (CUF). An external one piece "top hat" type heat spreader is attached to the backside of the die and substrate using high thermal conductivity epoxy.

STATS ChipPAC's Flip Chip FBGA packages are available in ball counts ranging from 32 to 900, body sizes from 4 x 4mm to 17 x 17mm and various package formats.

Flip Chip interconnection provides the ultimate in miniaturization, reduced package parasitics and enables new paradigms in the area of power and ground distribution to the chip which are not feasible with other traditional packaging approaches. STATS ChipPAC offers full turnkey services ranging from design through production, including high speed, high pin count digital and RF testing.

APPLICATIONS

Devices for wireless and portable products such as microprocessors, RFICs and power/analog ICs driven by miniaturization and low package parasitics.

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SPECIFICATIONS

Package Thickness	0.65 – 1.4mm
Die Thickness	6" 100–660µm (4–26mils) 8" 100–760µm (4–30mils) 12" 100–810µm (4–32mils)
Bump Pitch	150µm solder bump in production 140µm minimum normal solder bump qualified 80µm minimum Cu column bump
Marking	Laser

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 3 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

THERMAL PERFORMANCE

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Perf. ja θ°C/W
fcLFBGA	7 x 7	191	4.46 x 5.65	33.2
fcLFBGA-H*	14 x 14	425	4.9 x 4.9	14.0
fcLGA	13 x 13	144	5.5 x 5.5	27.7
	5 x 6	71	3.8 x 5.0	35.6

Notes: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2. *H/S: 0.3mm formed "Hat" type; 100um TIM1 and 100um lid adhesive: 1.75W/mK.

ELECTRICAL PERFORMANCE

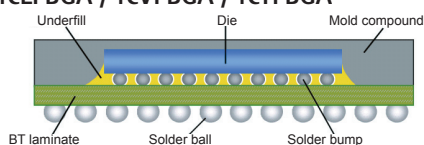
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz.

Package	Body Size	Die Size	Length	Inductance (nH)	Capacitance (pF)	Resistance (mΩ)
fcLFBGA	13 x 13mm	6.0 x 8.0mm	Self (short)	0.89	0.65	18.3
			Mutual	0.24	0.11	
			Self (long)	1.78	0.73	32.5
			Mutual	0.51	0.12	

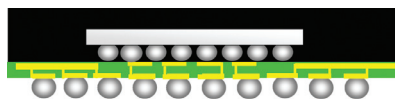
Note: Net = Total Trace Length + Via + Solder Ball.

CROSS-SECTIONS

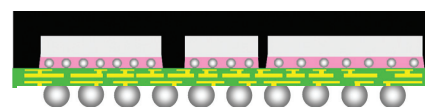
fcLFBGA / fcVFBGA / fcTFBGA



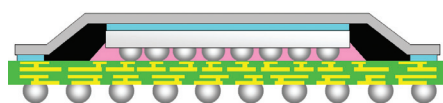
fcTFBGA with MUF



fcVFBGA-SS3



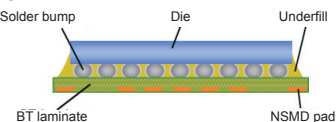
fcLFBGA-H



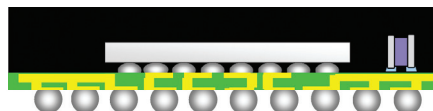
fcTFBGA-SD2



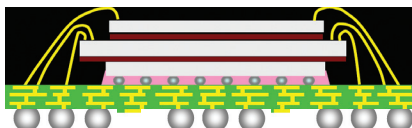
fcLGA



fcFBGA-SiP



fcTFBGA-SD3



fcTFLGA-SiP-SS3



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