Flip Chip BGA

fcBGA, fcBGA-SiP, fcBGA-H, fcBGA-MP

HIGHLIGHTS

- High performance packages up to 55mm body size with >3213 pins and thermal solutions ranging from bare die, stiffener only and one/two piece heat spreader
- ABF buildup to 6-2-6; minimum core thickness down to 200µm; coreless substrate and grounded lid for high electrical performance
- Packaging solution for Eu/LF bumped 28N/32N node with Extra/Ultra Low K die-electric
- "Green" flip chip solution with Pb-free, Cu column bump and halogen-free material sets

FEATURES

- 65N/Low K, 40N/ELK, and 28/32N ELK/ULK
- Eutectic, High Pb, Pb-free and Cu column
- Nitride, Polyimide, PBO wafer passivations
- Ni-Au, Ni-Pd-Au, SOP (solder-on-pad), OSP (organic solderable preservative), Ni-free SOP pad and immersion Sn finish
- Bumped wafer thinning down to 100µm for non-molded fcBGA
- 200mm (printed, plated) and 300mm (plated) bumped wafers; RDL with 200mm and 300mm bumped wafers
- Seamless integration of flip chip, SMT and in-line open/short testing operations
- F/A metrology tools for rapid diagnostics and debugging, including TDR, CSAM, X-ray, Ion milling and SEM
- All packages qualified to JEDEC specifications and/or custom requirements based on end applications

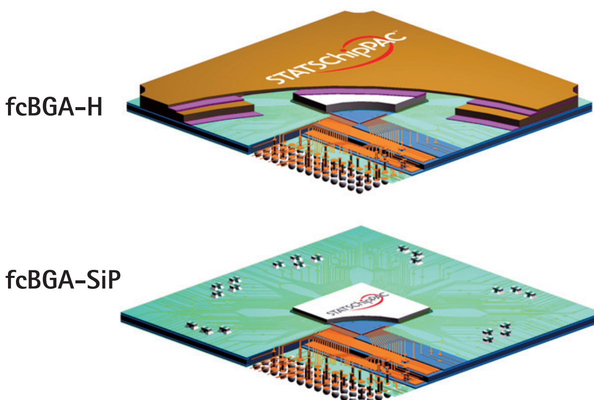
DESCRIPTION

STATS ChipPAC's high-end BGA Flip Chip packages include the fcBGA, fcBGA-SiP, fcBGA-H, fcBGA-MP and fcBGA-SS2/SS3. The fcBGA package is the main platform in this package sub-group, which also includes a thermally enhanced version with heat spreader (fcBGA-H) and a package subsystem meeting the standard BGA footprint that contains multiple components within the same package (fcBGA-MP). STATS ChipPAC's Flip Chip BGA packages are available in ball counts ranging from 220 to 3213, body sizes from 12 x 12mm to 55 x 55mm and various package formats.

Flip Chip interconnection provides the ultimate in miniaturization, reduced package parasitics and enables new paradigms in the area of power and ground distribution to the chip which are not feasible with other traditional packaging approaches. STATS ChipPAC offers full turnkey services ranging from design through production, including high speed, high pin count digital and RF testing.

APPLICATIONS

- ASIC and FPGAs requiring high pin counts and electrical performance
- CPUs driven by electrical performance
- GPU (Graphics Processing Units) requiring electrical performance and efficient on-chip power distribution
- PC chip sets and integrated graphics devices (IGP) driven by high I/O density
- Tablet application processor (AP) devices driven by small form factor with high I/O density



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SPECIFICATIONS

Die Thickness	6" 100-660µm (12-26mils) 8" 100-760µm (12-30mils) 12" 100-787µm (12-31mils)
Bump Pitch	Minimum 125µm area array
Marking	Laser
Packing Options	JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 4 or 3 (peak temp 230°, 245° or 260°)
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

THERMAL PERFORMANCE

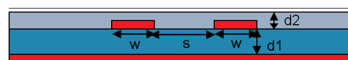
Body Size (mm)	Ball Count	Die Size (mm)	θjc (°C/W)	θja (°C/W) Natural Convection	1 m/s	2 m/s
31	792	9.6	1.1	14.0 / 10.0*	11.8 / 6.0*	11.0 / 5.7*
35	964	11.1	0.8	12.5 / 8.9*	11.0 / 5.5*	10.0 / 5.2*
40	1161	12.8	0.6	11.2 / 8.0*	9.4 / 4.8*	8.4 / 4.4*
40	1417	15.1	0.4	10.7 / 7.6*	8.7 / 4.3*	7.7 / 4.0*
45	1732	17.4	0.3	9.0 / 6.5*	7.5 / 3.9*	6.5 / 3.5*

Notes: *Includes heat sink (0.5" tall, channel design). Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2 or forced convection defined in JESD51-6.

ELECTRICAL PERFORMANCE

Parametric Data: Sample Embedded Micro-Stripline Configuration

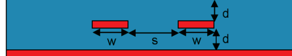
Metal Thickness	Prepreg Thickness(d1)	Solder Mask Thickness(d2)	Trace Width(w)	Trace Spacing(s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GHz	Diff. Pair Lossy Zdiff@1GHz	Lossy Propagation Delay Even Mode	Odd Mode
15µm	40µm	35µm	25µm	25µm	0.408	0.109	69.9Ω	84.1Ω	6.10ps/mm	6.54ps/mm
				40µm	0.414	0.097	70.9Ω	100.4Ω	6.12ps/mm	6.39ps/mm



Conductor material = copper
Prepreg material dialetric constant = 3.4@1GHz
Solder mask material dielectric constant = 3.9@1GHz

Parametric Data: Sample Stripline Configuration

Metal Thickness	Prepreg Thickness(d)	Trace Width(w)	Trace Spacing(s)	Inductance (nH/mm)	Capacitance (pF/mm)	Ind. Trace Lossy Z11@1GHz	Diff. Pair Lossy Zdiff@1GHz	Lossy Propagation Delay Even Mode	Odd Mode
15µm	40µm	25µm	25µm	0.323	0.126	54.6Ω	81.6Ω	6.37ps/mm	6.46ps/mm
			50µm	0.329	0.117	55.5Ω	99.0Ω	6.38ps/mm	6.40ps/mm



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PACKAGE CONFIGURATIONS

Package Size (mm)	Ball Count	Bump Pitch (µm)	Bump Count	Substrate	Layer
12	481	220	832	B/U	6L
14	493	187	716	B/U	4L
15	220	187	861	B/U	8L
	196	180	518	B/U	6L
17	256	225	246	B/U	8L
18	1225	150	4724	Laminate	6L
21	400	225	960	B/U	6L
	624	156	1086	B/U	6L
23	548	180	726	B/U	6L
25	900	150	3441	B/U	6L
27	540	180	896	B/U	4L
	732	180	1028	B/U	4L
	880	140, 180	4382	B/U	4L
29	780	200	2776	B/U	6L
	969	170	1129	B/U	6L
31	701	225	1271	B/U	8L
	736	340	976	Laminate	4L
	841	200	1624	B/U	8L
	864	125	2539	B/U	4L
	899	150	2796	B/U	6L
	900	150	1857	B/U	6L

Package Size (mm)	Ball Count	Bump Pitch (µm)	Bump Count	Substrate	Layer
33	1024	174	1445	B/U	12L
35	937	140	4382	B/U	4L
	956	225	2700	B/U	6L
	960	340	1935	Laminate	4L
	960	225	2703	B/U	6L, 8L
	1017	160	3284	B/U	8L
	1089	200	2575	B/U	8L
	1156	150	5590	B/U	8L
40	1004	250	2116	B/U	8L
	1012	225	3138	B/U	8L
	1413	225	3599	B/U	8L
	1517	150	8055	B/U	12L
	1520	180	7550	B/U	10L
42.5	1677	225	4488	B/U	8L
	1681	170	7336	B/U	8L
45	1728	225	4899	B/U	8L
	1920	200	6477	B/U	12L
	1935	180	7550	B/U	12L
55	2915	180	7550	B/U	12L
	3213	150	7358	B/U	14L

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March 2012