

# eWLB

## Embedded Wafer-Level Ball Grid Array

### HIGHLIGHTS

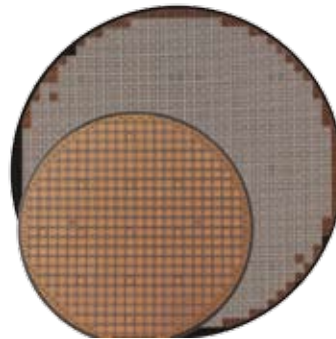
- Combines traditional front-end and back-end manufacturing techniques with parallel processing of all chips on the wafer
- Batch processing increases throughput and reduces manufacturing costs
- Elimination of substrate simplifies supply chain and reduces cost
- Provides the performance of fan-in WLP but decouples die from package size for greater flexibility
- Enables a dramatically higher number of external contacts as compared to fan-in WLP
- 1 and 2 sided PoP versions with total height <1.0mm
- MCP versions with IPD integration capability

### FEATURES

- No substrate required resulting in a thinner package with lower warpage
- Unique structure allows thinnest advanced package profile and excellent 2D and 3D integration platform
- Miniaturized high performance package
- Green packaging (Pb-free and Halogen-free)
- Cu/low-k (ELK) compatible packaging technology
- Batch process of wafer level including wafer-level test
- Embeds die in mold during assembly/packaging
- Supports incoming wafers in both 8" and 12" diameters
- No bumping required
- Low packaging and test costs due to batch process
- Excellent electrical and thermal performance
- Simple logistics and supply chain (no substrate, bumping, etc.)

### APPLICATIONS

eWLB is uniquely suited to a wide and growing range of applications including baseband, RF, power management, analog and other emerging applications for mobile, connectivity, MCU, networking and consumer applications.



200mm and 300mm eWLB wafers

### DESCRIPTION

Embedded Wafer-Level Ball Grid Array (eWLB) technology is an enhancement of standard wafer-level packages (WLPs) that was developed to provide a solution for semiconductor devices requiring a higher integration level and a greater number of external contacts. eWLB technology uses a combination of traditional 'front-end' and 'back-end' semiconductor manufacturing techniques which greatly reduces manufacturing costs while providing a smaller package footprint with higher input / output (I/O) along with increased thermal and electrical performance.

eWLB is a Fan-Out WLP (FO-WLP) as opposed to a more conventional Fan-In WLP (FI-WLP). Unlike FI-WLP, eWLB ball pitch and I/O count are not limited by the die size because its package size is decoupled from die size, allowing it to accommodate die shrinks and larger ball pitches that would not fit within the die area of a FI-WLP. Special materials also extend the eWLB package size and ball count beyond FI-WLP capabilities while still meeting board level reliability requirements. This allows for a broader application range for the eWLB to larger size and ball count mobile and consumer devices, while still offering the advantages of WLP related to performance, simple logistics and supply chain, lead-free/halogen-free and compatibility with advanced wafer fabrication nodes.

Backed by a strong infrastructure and cost effective manufacturing process, STATS ChipPAC offers a high performance solution at a lower cost point with volume and maturity, leveraging the potential of batch panel processing of high density wafer fabrication redistribution technology. STATS ChipPAC has established a robust eWLB high volume manufacturing process with automated wafer reconstitution (including wafer-level molding), redistribution using thin film technology, solder ball mount, package singulation and testing. Incoming wafers in both 200mm and 300mm diameters can be supported. No bumping is required as the eWLB package is essentially built on top of a reconstituted wafer.

## SPECIFICATIONS

<b>Package Thickness</b>	0.5 - 0.8mm
<b>Bump Pitch Range</b>	0.4 - 0.5mm
<b>Bump Height</b>	0.2 / 0.23mm (0.4 / 0.5mm pitch)
<b>Backside Coating</b>	Laminated coating (optional)
<b>Marking</b>	Laser marking
<b>Inspection</b>	Automatic optical inspection with electronic wafer mapping
<b>Packing Options</b>	Fully automated die pick/place into custom pocket tape/reel or wafer pack media

## RELIABILITY

<b>Moisture Sensitivity Level</b>	MSL1 @ lead free condition (260°C)
<b>Temperature Cycling</b>	-40°C/125°C, 850 cycles -25°C/100°C, 1000 cycles
<b>High Temperature Storage</b>	150°C, 1000 hrs
<b>Unbiased HAST</b>	130°C/85% RH, 96 hrs
<b>Temperature Humidity Bias Test</b>	85°C/85%/5V, passed 1000 hrs
<b>TC on Board</b>	-40°C/125°C, 2 cycles/hr, passed 500 cycles
<b>Multiple Solder Reflow</b>	5x, 10x and 20x reflows with minimal reduction in bump shear strength
<b>Drop Test</b>	Passed JEDEC drop test for 8 x 8mm, 183 balls (0.5mm pitch)

## THERMAL PERFORMANCE $\theta_{ja}$ (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Body Size (mm)	Die Size (mm)	Thermal Performance $\theta_{ja}$ (°C/W)	Thermal Vias (on test board)
8 x 8	5 x 5	32.5	simulation data

Notes: Thermal performance in the 20-40°C/W range without thermal enhancement. Application specific thermal characterization available upon request.

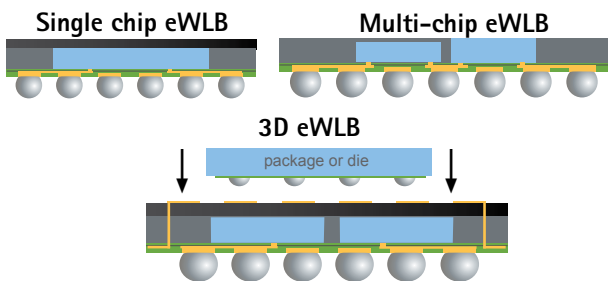
## ELECTRICAL PERFORMANCE

- Dependent on application design, but capable to beyond 60GHz
- Application specific electrical characterization available upon request
- Thick Cu for high current low inductance applications

## PACKAGE CONFIGURATIONS

- Body sizes (mm): 2.2 x 2.2 – 12 x 12 and expanding (package size dependent on die size)
- Multiple die: Two (side-by-side) and expanding
- 3D eWLB with vertical interconnects (1 and 2 sided versions)
- IPD integration in standard as well as MCP versions

## CROSS-SECTIONS



## NEXT-GENERATION eWLB

The next generation of eWLB technology leverages the success of first-generation eWLB (single metal RDL on the bottom side of the eWLB package), with focused development on multi-metal layer RDL, multiple die side-by-side (>2), extension of package size to <2x2mm and >14x14mm, reduction of package thickness to <0.5mm and smaller (including leadless land grid array version), RLC-IPD, heterogenous integration and eWLB-PoP technologies. eWLB is also ideally suited to 3D applications such as SiP and other 3D configurations using STATS ChipPAC's TSV technology. In addition, STATS ChipPAC is actively working with technology partners to further extend eWLB capabilities to meet the needs of a broader set of advanced applications.

## eWLB PROCESS FLOW

- 1) Reconstituted wafer**
  - Wafer saw and pick-and-place from incoming wafer
  - Probed good die
  - Molded reconstituted wafer using proven materials
  - Molded artificial wafer starting point for thin film technology
- 2) Redistribution**
  - Thin film technology with advanced design rules
  - Standard thin film equipment
  - Proven and reliable material set
- 3) Ball Mount and Singulation**
  - Standard back-end assembly flow (and equipment)
- 4) Test, Mark, Scan, Pack**
  - Standard or wafer level-based test flow
  - Standard assembly



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