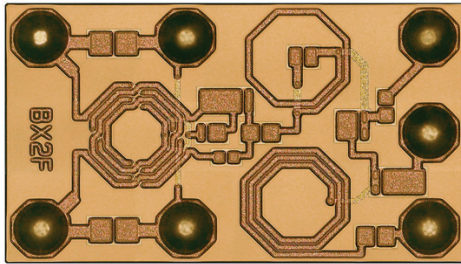
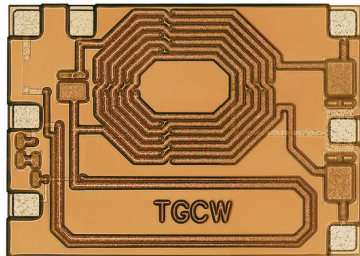


IPD

Chip Scale Module Package - Integrated Passive Device



WiMAX
Balanced Filter



GSM
Balun & Coupler

FEATURES

- Embedded RLC components with excellent performance
- Resistors to 100,000 ohms
- Capacitors range: 0.2pF-100pF
- Inductors to 30nH
- IPD duplexers, filters for wireless applications
- Compact baluns for RF applications
- Computerized component generation for fast flawless design (1st run silicon success is typical)
- Library RLC components, filters and baluns for GSM, DCS, PCS, GPS, WiMAX and WLAN a/b/g
- Full electrical models of all library components
- Full foundry services available
- Foundry matrix mask space available
- Packaging available in QFN, FBGA, FLGA and eWLB formats

APPLICATIONS

- RF Power Amplifier Matching/Filters/Couplers
- Front End Modules (FEM)
- GSM/DCS and CDMA cellular phones
- Wireless LAN 802.11 a/b/g and WiMAX systems
- 802.11a/b/g and WiMAX filters
- GPS Systems
- Functional Interposers
- Baluns from 750MHz-6GHz
- Multi-band RF Transceivers
- Miniaturization of RF Systems

DESCRIPTION

Chip Scale Module Packaging (CSMP) is an advanced system-in-package (SiP) solution which features a modular architecture that integrates mixed IC technologies and a wide variety of passive devices (IPD) such as resistors, capacitors, inductors, filters, baluns, transceivers, receivers and interconnects directly onto a silicon substrate. The result is a high performance system level solution, which provides a significant reduction in die size, weight, number of interconnections and system board space requirements, and can be used for many applications.

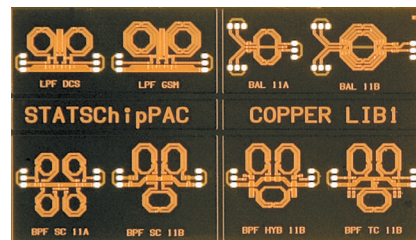
Enabling IPD Technology

STATS ChipPAC's IPD technology is a key enabler of its innovative CSMP offering which features silicon-based passive integration of RLC components. IPDs are a cost effective way to reduce footprint, reduce interconnection complexity, improve component tolerance, yield and reliability. By integrating and fabricating passive devices at the silicon wafer level, STATS ChipPAC is able to fabricate IPDs which are significantly smaller, thinner and with higher performance than standard passive devices.

To achieve superior IPD performance, STATS ChipPAC employs a copper metallization process capable of depositing 8 microns or more of copper on a silicon wafer. This results in higher Q components that reduce loss in the RF signal transmission path, thereby increasing battery performance of the wireless system and improving reception. The size of matching circuitry and filters is often reduced by 40%.

IPD Component Library

STATS ChipPAC's foundry service includes fully characterized resistor, capacitor, inductor, filter and balun libraries, complete with full electrical models of all library components for packages such as QFN, FBGA, FLGA and eWLB. In addition to standard IPD library solutions, customized IPD designs are also available. Refer to the *IPD Products Databook* (2nd edition) for a comprehensive list of IPD products that can be integrated into RF SiP solutions.



Sample
Filter
Library

A Comprehensive RF Solution

STATS ChipPAC provides the highest level integration of wireless systems. With leading edge technology in CSMP, IPD, eWLB, 3D packaging and a comprehensive RF solutions portfolio, including wafer sort, design, assembly, RF test and supply chain management, STATS ChipPAC offers RF semiconductor companies a complete turnkey solution and distinct competitive advantage in their market.

Chip Scale Module Package - Integrated Passive Device

SPECIFICATIONS

Die Thickness	250µm (nom)
Gold Wire	1.0mil
Marking	Laser mark (black or white)
Packing Options	JEDEC tray / tape and reel

THERMAL PERFORMANCE, θ_{ja} (°C/W)

Package	Body Size (mm)	Die Size (mm)	Simulated Values θ_{ja} , C/W
230 FBGA-CSMP	15 x 15mm (2L)	7.5 x 8.0	24.9
104 fcFLGA-CSMP	15 x 15mm (4L)	10.5 x 10.5	23.6

Notes: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7, JESD51-9) under natural convection as defined in JESD51-2

RELIABILITY

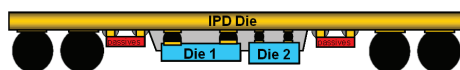
Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C/150°C, 1000 cycles
UHASt (laminated package)	130°C, 85% RH, 96 hrs
High Temperature Storage	150°C, 500 hrs
Pressure Cooker Test (WLCSMP)	121°C 100% RH, 2 atm, 168 hrs
Liquid Thermal Shock	-65°C/150°C, 500 cycles

ELECTRICAL PERFORMANCE

Package	Body Size (mm)	Frequency	SPICE Model or S-Parameter
230 LFBGA-CSMP	15 x 15mm (2L)	100MHz or 1.0GHz	Values are influenced by final design
104 fcFLGA-CSMP	15 x 15mm (4L)	100MHz or 1.0GHz	Values are influenced by final design
eWLB RDL	6 x 6mm (1L or 2L)	100MHz or 1.0GHz	Values are influenced by final design

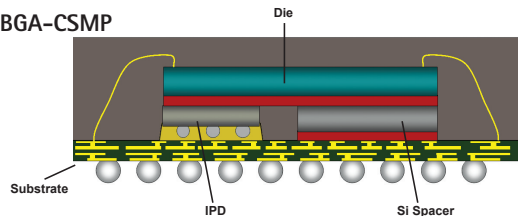
CROSS-SECTIONS

WLCSMP (Wafer-Level Chip Scale Module Package)

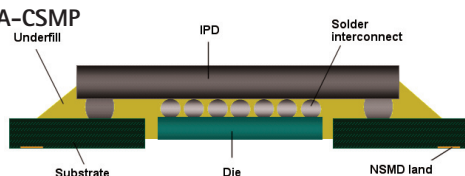


Module Size	10 x 10 x 1.0mm, 38 I/O
Ball Pitch	0.8mm
Ball Diameter	0.55mm minimum
IPD Tile	10 x 10 x 0.45mm
FC Die	3x
0201 Passives	6x

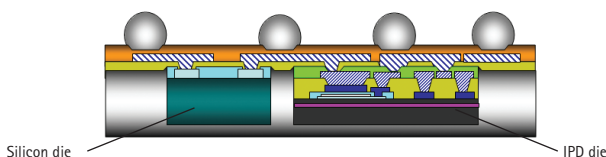
FBGA-CSMP



fcFLGA-CSMP



IPD integrated in eWLB with Silicon IC



PACKAGE CONFIGURATIONS

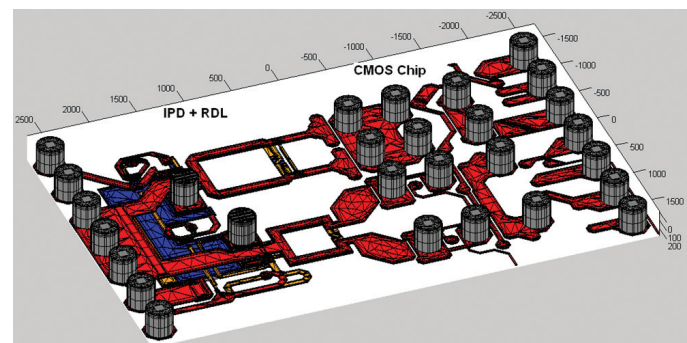
FBGA-CSMP – LFBGA packages with body sizes up to and including 15 x 15 sq. mm. Refer to STATS ChipPAC's FBGA datasheet.

FLGA-CSMP – FLGA packages with body sizes up to 15 x 15 sq. mm. Refer to STATS ChipPAC's FLGA datasheet.

WLCSMP – CSMP package with body size of 10 x 10 sq. mm.

eWLB – IPD integrated in eWLB package with body size of 6 x 6 sq. mm or less.

IPD – Standalone IPDs (balun, diplexer, LPF, BPF, etc.) for RF applications. Refer to STATS ChipPAC's *IPD Product Databook* (2nd ed.) for a complete product list.



A sample eWLB module containing a CMOS power amplifier chip (on the right) and an IPD chip (on the left). The IPD chip is used for matching and filtering functions. The interconnection between the CMOS chip and the IPD chip is made by RDL through the eWLB process.

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