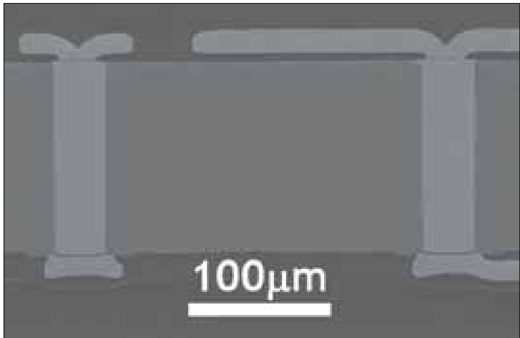
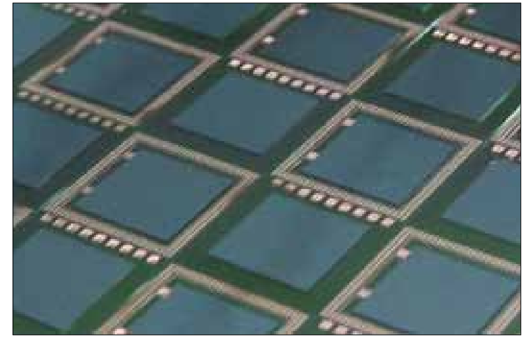
Through Silicon Via (TSV)



3D TSV with fine via



Chip-to-Wafer bonding for 2.5D/3D TSV

Highlights

- **Enabling 3D package for low power, high performance devices in mobile market**
- **Combined with microbump bonding and advanced flip chip technology, 2.5D TSV technology delivers a high performance solution for computing and networking applications**
- **Greater space efficiencies compared with traditional wirebonding and flip chip stacking by means of face-to-back and face-to-face bonding**
- **Higher interconnect density**

STATS ChipPAC TSV CAPABILITIES

TSV Post-Process (mid-end)

- Bumped wafer thinning and planarization
- Temp bonding/de-bonding
- Backside via reveal
- Dielectric deposition
- Silicon recess and backside metallization
- Thin wafer with TSV handling and dicing
- Microbump technology for 50/40um u-bump plating

TSV Assembly/Packaging (back-end)

- Chip-to-Wafer or Chip-to-Chip attachment options
- Fine pitch microbump bonding (solder, Cu column)
- Wafer level underfill (ultra small gap underfill process)
- TSV package reliability and characterization
- Developing Next-Generation 3D TSV packaging

TSV Silicon Interposer Technology

- First and easier step for TSV application
- Qualified tapered TSV process for low density Si interposer (sub-200um pitch)
- High density Si interposer with TSV in joint development
- Potential to replace high-end organic (BU) substrates
- Thinner profile, tighter pitch and high thermal/electrical performance

A Pioneer in TSV Technology

As a longstanding leader in 3D packaging, STATS ChipPAC was one of the first Outsourced Semiconductor Assembly and Test (OSAT) providers to invest in TSV technology with a 51,000 sq. ft. R&D facility in Woodlands, Singapore dedicated to the development of next-generation wafer-level integration with TSV technology. STATS ChipPAC has developed and qualified key technology in areas such as TSV formation and metallization, bumped wafer thinning, thin wafer handling, 3D microbump bonding, wafer-level underfill and TSV assembly. New state of the art process equipment and metrology tools were installed in 2011 as part of a high volume manufacturing expansion of 300mm wafer capability, bringing TSV into volume production mode. Additional expansion beginning in 2012 will further increase volume and quality levels of all advanced wafer scale products including TSV.

TSV is an important developing technology that utilises short, vertical electrical connections or "vias" that pass through a silicon wafer in order to establish an electrical connection from the active side to the backside of the die, thus providing the shortest interconnect path and creating an avenue for the ultimate in 3D integration. TSV technology offers greater space efficiencies and higher interconnect densities than wirebonding and flip chip stacking. When combined with microbump bonding and advanced flip chip technology, TSV technology enables a higher level of functional integration and performance in a smaller form factor.

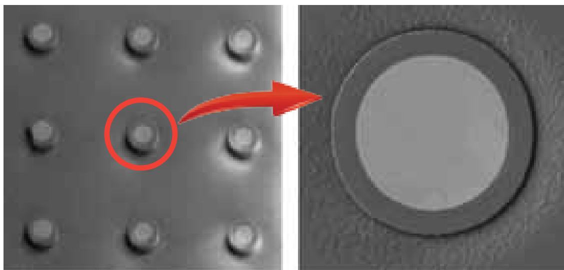
TSV Assembly / Packaging

STATS ChipPAC has full front to back-end manufacturing capabilities and currently handles both chip-to-chip (C2C) and chip-to-wafer (C2W) assembly for TSV technology. This includes high density microbump capabilities in both solder and copper column, microbump bonding down to 40um pitch, thin wafer handling, wafer-level underfill, thin wafer dicing and microbumps for flip chip interconnection. Microbump technology is critical to delivering fine pitch, low profile solutions for high performance devices.

Through Silicon Via (TSV)

TSV Mid-End Fabrication

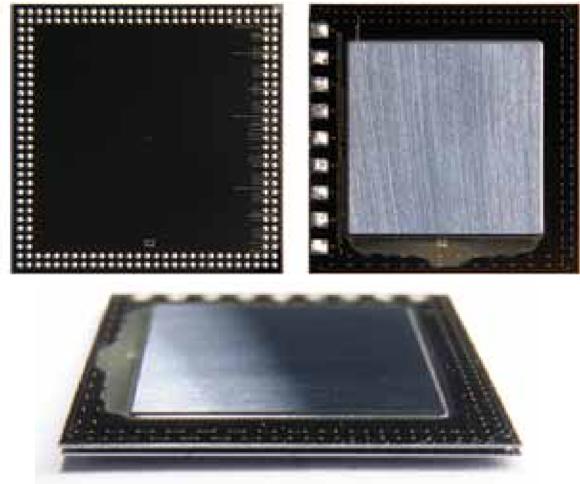
STATS ChipPAC also offers a 300mm post-TSV "mid-end" fabrication process flow that occurs between the wafer fabrication and back-end assembly process. Mid-end processes support the advanced manufacturing requirements of 2.5D and 3D TSV, as well as wafer-level packaging, flip chip and embedded die technology. The mid-end process includes temporary bonding/de-bonding, wafer thinning and planarization, back-side via reveal, silicon recess and back-side metallization and microbumping. Microbump is required to meet fine pitch, low profile applications in 3D TSV, stacking and assembly. STATS ChipPAC offers 40um pitch microbump bonding.



10um diameter Cu TSV reveal after thinning and CMP

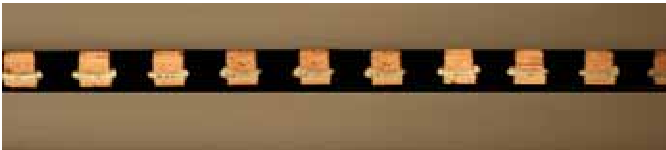
TSV Interposer and Assembly

STATS ChipPAC offers TSV interposer fabrication to provide a "bridge" between today's 2D packaging solutions and next-generation 3D technology. Often referred to as 2.5D technology, TSV interposers are an efficient and practical approach to die level integration.

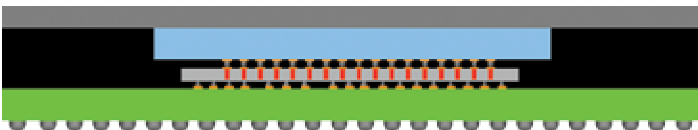


3D stacked TSV interposer

TSV Assembly Package Options



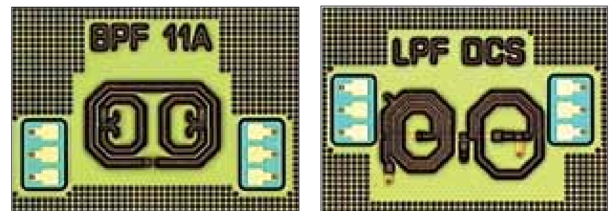
Thermal Compression bonded (TCB) micro-bumps on the TSV tips in fcFBGA

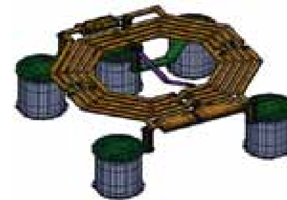


TSV in fcFBGA

TSV in IPD

- Adding TSV to the IPD structure results in a unique high functionality solution
- Performance and margin improvements result from increased distance between IPD surface and ground plane





GSM Balun IPD with TSV

CONTACT US

For more information about STATS ChipPAC's TSV capabilities, contact us at *salescontact@statschippac.com.*

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