

The Market Leader in eWLB Technology



As the world demand for portable electronics has accelerated, the need to make semiconductors smaller, faster, lighter and cheaper has never been greater. Consumers are looking for portable devices that have the most features and functionality in the smallest size possible and at a price they are willing to pay. At STATS ChipPAC, we offer advanced, leading edge manufacturing and testing solutions for mobile applications with embedded Wafer-Level Ball Grid Array, or eWLB, technology.

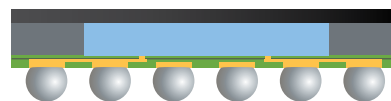
What is eWLB technology?

Embedded Wafer Level Ball Grid Array (eWLB) technology is a semiconductor packaging approach where an integrated circuit (IC) is assembled directly on a reconstituted wafer instead of the traditional process of dicing up the ICs on the wafer and putting the individual die in a plastic package. eWLB offers small package dimensions, improved electrical and thermal performance, and maximum connection density for wireless applications.

Advanced fab technology nodes drive smaller silicon die sizes with finer interconnect pitches. The eWLB design advantage is that the package size is larger than the silicon die in order to provide sufficient area for the interconnection of the package to the application board. As a result, eWLB has the potential to realize a higher number of interconnects with standard pitches at multiple wafer technology nodes.

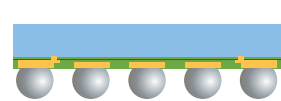
STATS ChipPAC has rapidly ramped this advanced technology to high volume production and established a clear leadership position in the industry in terms of manufacturing volume, capacity and yields.

Fan-Out WLP (eWLB)

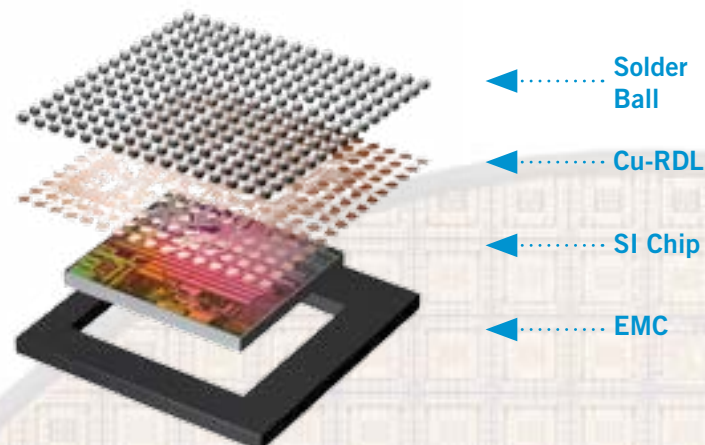


Interconnects independent
of chip footprint

Fan-In WLP



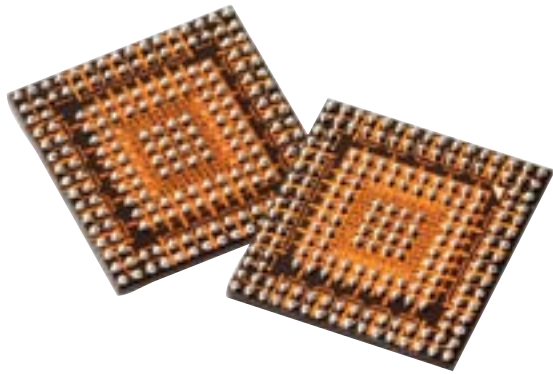
Interconnects only
under chip footprint



The eWLB advantage

eWLB technology provides significant performance, size and cost benefits compared to other packaging technology available today. The benefits of eWLB include:

- Smaller and thinner package solution as compared to conventional leadframe and laminate packages
- Greater flexibility in package sizes due to fan-out wafer level packaging design
- Robust package with strong thermal and electrical performance offering a high-performance, power-efficient solution
- Superior reliability for mobile applications
- Enables a dramatically higher number of input/output count as compared to fan-in wafer level packages
- Elimination of package substrate and wafer bumping simplifies logistics and supply chain costs
- Batch processing increases throughput and reduces manufacturing costs



Cost effective 300mm manufacturing

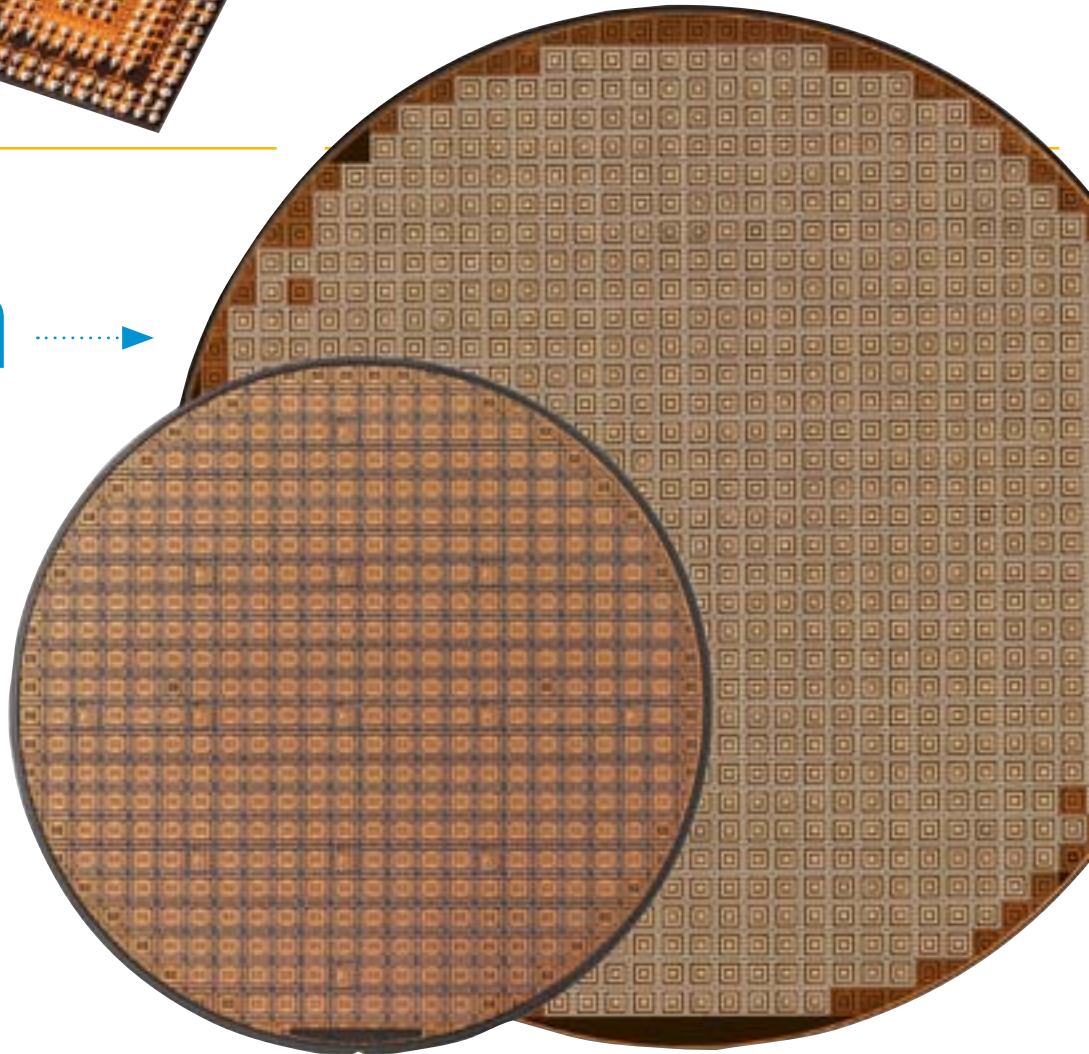
STATS ChipPAC's robust, automated eWLB manufacturing process which includes wafer reconstitution, wafer level molding, redistribution using thin film technology, solder ball mount, package singulation and testing has proved to be a solid foundation on which the company has rapidly ramped production volumes. STATS ChipPAC was the first company to achieve high volume production of eWLB technology and today is shipping millions of eWLB units per week.

STATS ChipPAC has also led the industry in transitioning from 200mm to 300mm reconstituted wafer manufacturing for eWLB. The transition from 200mm to 300mm eWLB wafer manufacturing provides STATS ChipPAC and its customers with a number of cost and productivity benefits such as higher efficiency and economies of scale as compared to the original 200mm eWLB reconstituted wafer format.

Reconstituted Wafers

300mm▶

200mm▶

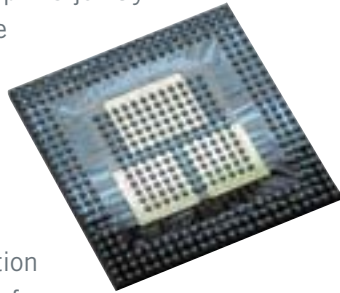


Pioneering next-generation eWLB technology

With smaller silicon chips and extremely fine pitch requirements, the challenge arises of how to maintain or even increase the number of input-output contacts, while keeping the semiconductor package compact, slim, light, high performing and cost effective. Next-generation eWLB technology utilizes both sides of a reconstituted wafer to provide solutions for semiconductor devices with a higher integration level and a greater number of contact elements.

Through an exclusive alliance with its technology partners, STATS ChipPAC jointly developed and is the first in the semiconductor industry to manufacture innovative eWLB technology such as:

- side by side devices
- ultra thin eWLB packages
- multi-metal layer redistribution
- and two-sided redistribution for 3D packaging



At STATS ChipPAC, development work continues on the eWLB evolution to enable larger package sizes, higher Input/Output (I/O) density and 3D Package on Package (PoP) solutions to address a wider applications market.

Ideal applications

Advanced wafer level technologies like eWLB are essential to support our customers' requirements for increased performance and functionality in a smaller footprint for sophisticated mobile devices such as smartphones and tablets. eWLB technology is successfully enabling semiconductor manufacturers to provide a high performance, cost effective solution for mobile and consumer applications. Today the single largest demand for eWLB is in mobile phone devices such as:

- Baseband processors
- RFIC / RF transceivers
- Connectivity devices (WiFi, BT, GPS)
- PMIC
- CMOS PA / module

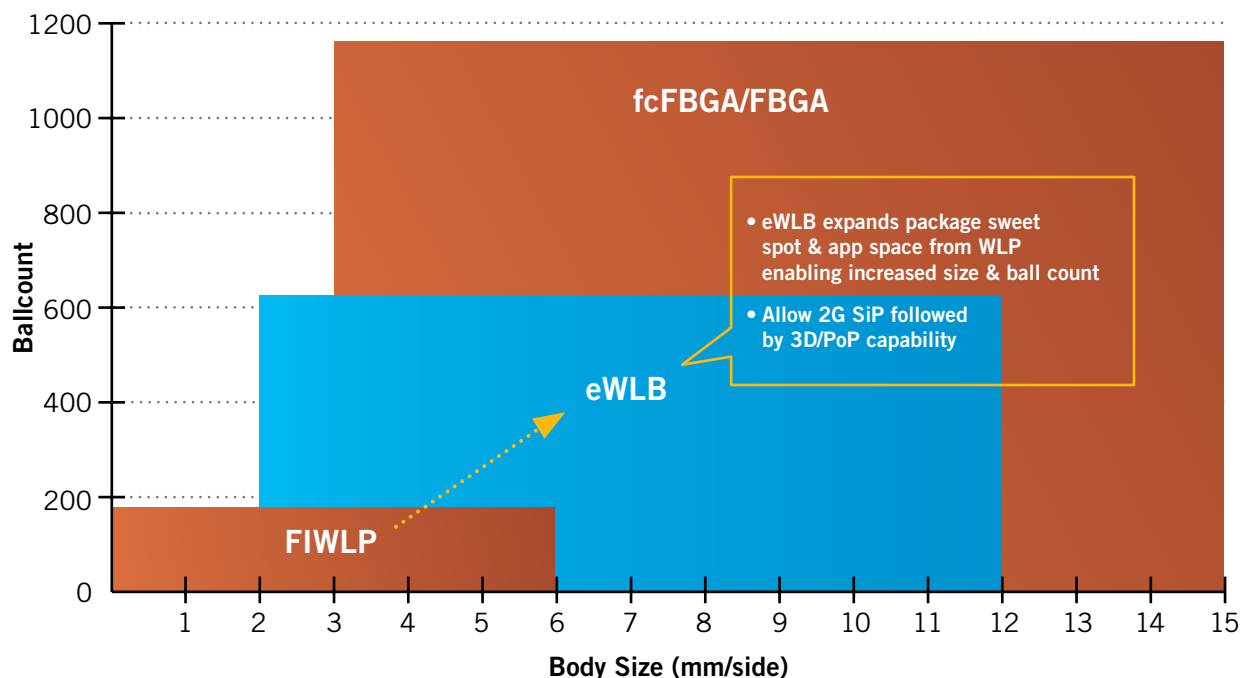


Demand for eWLB is also rapidly growing in other market segments such as:

- Digital cameras and camcorders (analog FE, controllers)
- Portable gaming devices, media players, readers

eWLB technology is quickly becoming the new advanced packaging solution that more customers are choosing for complex and power efficient semiconductor devices in mobile phones and other handheld electronic products. To find out more about eWLB, visit us online at www.statschippac.com.

eWLB Application Space





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A partial view of a microchip die pattern is visible in the bottom-left corner of the page, mirroring the pattern seen at the top.