

Flip Chip with Cu Column, BOL and Enhanced Processes

HIGHLIGHTS

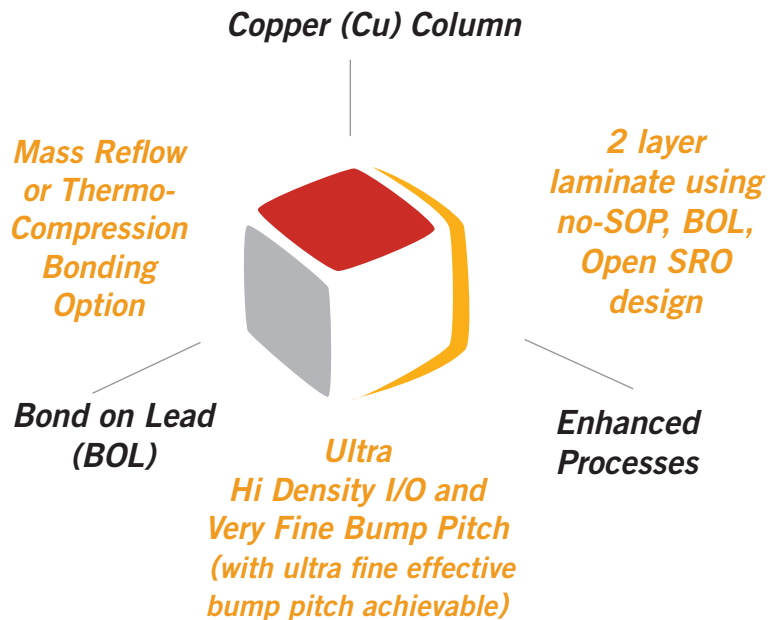
- Copper (Cu) column with Pb-free cap
- Patented, routing-efficient Bond on Lead (BOL) interconnection structure and optimized bump layout help "fit" flip chip designs into low cost laminate substrates
- Mechanics of BOL interconnect structure eliminates ELK / ULK damage on advanced Si node devices despite use of Cu column (Pb-free) bump metallurgy and dense routing
- Finer effective bump pitches achievable through high routing efficiency of BOL technology
- Compatible with both Mass Reflow and Thermo-compression bonding for optimal cost, ultra fine pitch capability and design flexibility
- Scalable to high I/O density and fine bump pitch down to 40µm
- Capillary underfill (CUF) and Mold underfill (MUF) with Cu column bump process technology for higher throughput
- Elimination of Solder-on-Pad (no-SOP) and relaxation of line / space design rules offer lowest flip chip substrate cost
- Smaller package size and lower electrical parasitics compared to corresponding wirebond package options
- Superior electromigration life with Cu column bump
- Cost reduction of 10-30% over standard flip chip packages for most designs

FEATURES

- Bumped wafer thinning: 100µm Si thickness in production, 75µm qualified
- 0.40mm minimum package ball (BGA) pitch in production
- High density matrix strip for fcFBGA and wide boat format for singulated fcBGA
- Conventional 2/4 layer laminate, laminate build-up (BU) and ABF BU substrates
- In-house Cu column wafer bumping for 200 and 300mm wafers
- Ultra fine pitch capability: 150µm to 40µm bump pitch
- Mold underfill (MUF) and Capillary underfill (CUF) optional) with mass reflow or nonconductive paste (NCP) with thermo-compression bonding (TCB)
- Broad fab node compatibility: 180n, 65n-LK, 40/28/20/14n-ELK/ULK
- Applicable across broad package range: fcBGA /-H, fcFBGA /-H (fcCSP) and fcPoP (3D)
- Wide range of package body sizes: 7 x 7mm to 35 x 35mm

APPLICATIONS

fcCuBE™ is a compelling solution for a wide cross section of end products in the mobile/handheld, computing and high-end network/telecom markets, including devices for wireless and portable products such as RFICs and power/analog ICs driven by miniaturization and low package parasitics, and for ASIC, graphics, computing and networking products driven by superior electrical and thermal performance.



DESCRIPTION

STATS ChipPAC has taken its innovative Low Cost Flip Chip (LCFC) technology and enhanced it to achieve greater design flexibility and performance across a broader range of applications, I/O requirements and fab nodes. This enhanced technology has been renamed fcCuBE™ to better describe its broader range of enhanced features and capabilities.

fcCuBE™ technology leverages innovations such as copper (Cu) column bump, patented Bond-on-Lead (BOL) interconnection and enhanced assembly processes such as mold underfill (MUF) to deliver high input/output (I/O) density, performance and superior reliability in advanced silicon nodes while retaining the low price points which make it competitive with mainstream semiconductor packaging solutions available today. This combination of enhancements allows greater design flexibility utilizing relaxed substrate design rules and a streamlined manufacturing process.

fcCuBE™ packages are produced on substrates with matrix strip or singulated format, and use overmolding and saw singulation processes for strip base substrate similar to wirebond packages of the same form factor. The fcBGA is typically an exposed die package with CUF (capillary underfill); fcFBGA is typically an overmolded package; both fcBGA and fcFBGA use solder balls for second level (BGA) interconnection; fcFBGA-SDx represents a variation of fcFBGA comprising a "hybrid" stacked construction, i.e., flip chip die on the bottom and wirebond die on the top; while the fCLGA is an exposed die product that does not have solder balls.

STATS ChipPAC's fcCuBE™ packages are available in ball counts ranging from 32 to > 1000 depending on body size and external terminal (BGA) pitch. Other features such as heat spreaders for thermal enhancement, surface mounted passive components, etc. that are offered with traditional fcFBGA and fcBGA packages are also available for fcCuBE™ packages.

Flip Chip with Cu Column, BOL and Enhanced Processes

SPECIFICATIONS

Package Thickness	0.65-2.9mm
Die Thickness	200mm wafers: 100-710 μ m (4-28mils) 300mm wafers: 100-810 μ m (4-32mils)
Bump Pitch	fcFBGA 40/80 μ m (qualified) fcBGA 125 μ m (qualified)
Effective Bump Pitch	fcFBGA 40/80 μ m w/1 line btw bumps (qualified) fcBGA 62.5 μ m w/1 line btw bumps (qualified)
Marking	Ink or laser

RELIABILITY

Excellent reliability margins: passed 3000 cycles for TCB and 3000 hours for HTS (well above industry standard requirement of 1000x each)

Moisture Sensitivity Level	JEDEC Level 3 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiased HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

THERMAL PERFORMANCE

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation and/or measurement for specific cases should be performed for maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Perf. ja $\theta^{\circ}\text{C/W}$
fcLFBGA	7 x 7	49	4.6 x 5.0	46.0
fcLGA	13 x 13	144	5.5 x 5.5	27.7
fcBGA-H	35 x 35	1084	10.0 x 10.0	11.2/8.0* (8.4 / 4.4*)

Note: Simulation data based on package mounted to 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2; * represents cases with extruded Aluminium heat sink; numbers in parentheses are for 2 m/sec air flow and provided for reference for applications that provide fans or other forms of air flow in the system.

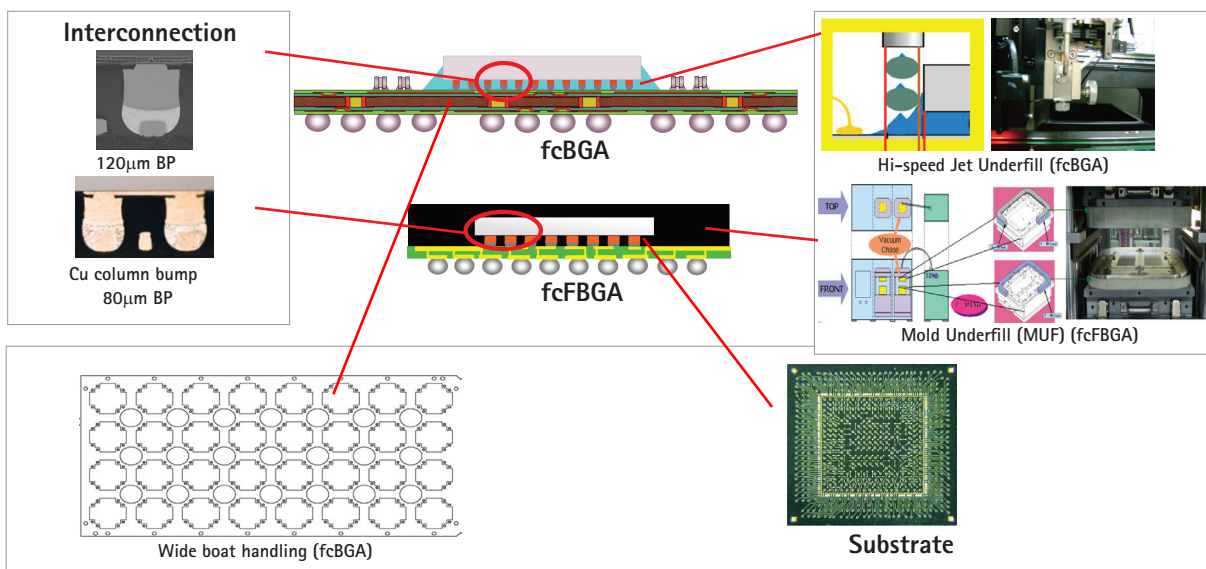
ELECTRICAL PERFORMANCE

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz.

Package	Body Size (mm)	Die Size (mm)	Length	Inductance (nH)	Capacitance (pF)	Resistance (m Ω)
fcLFBGA	13 x 13	6.0 x 8.0	Self (short)	0.89	0.65	18.3
			Mutual	0.24	0.11	
			Self (long)	1.78	0.73	32.5
			Mutual	0.51	0.12	

Note: Net = Total Trace Length + Via + Solder Ball.

CROSS-SECTIONS



Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823
Global Offices USA 510-979-8000 JAPAN 81-3-3507-5676 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
 KOREA 82-31-639-8911 TAIWAN 886-3-593-6565 SWITZERLAND 41-22-929-5658

The STATS ChipPAC logo is a registered trademark of STATS ChipPAC Ltd. Trademark registered in United States. Singapore company registration number 199407932D. All other product names and other company names herein are for identification purposes only and may be the trademarks or registered trademarks of their respective owners. STATS ChipPAC disclaims any and all rights in those marks. STATS ChipPAC makes no guarantee or warranty of its accuracy in the information given, or that the use of such information will not infringe on intellectual rights of third parties. Under no circumstances shall STATS ChipPAC be liable for any damages whatsoever arising out of the use of, or inability to use the materials in this document. STATS ChipPAC reserves the right to change the information at any time and without notice. ©Copyright 2012. STATS ChipPAC Ltd. All rights reserved. March 2012