“Improvement of ELK Reliability in Flip Chip Packages using Bond-on-Lead (BOL) Interconnect Structure“

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Abstract

In this paper, a novel flip chip interconnect structure called Bond-On-Lead (BOL) and its ability to reduce stress in the sensitive sub-surface ELK (Extra Low K) layers of the die is presented. BOL is a new low cost flip chip packaging solution which was developed by STATSChipPAC to dramatically reduce the cost of flip chip packaging. The BOL solution allows for efficient substrate routing by virtue of the use of narrow BOL pads and the removal of solder mask in the area of the BOL pads, which eliminates the limitations associated with solder mask opening sizes and positional tolerances. In addition to the compelling cost benefits, modeling results are confirmed with empirical reliability testing data to show that BOL is superior to the traditional Bond-on-Capture Pad (BOC) configuration from a mechanical stress and reliability perspective. The focus of this paper is on the theoretical analysis of the stress, strain, and warpage associated with the BOL configuration compared with the traditional BOC structure. For the package deformation, the global finite element method is used to simulate the package warpage. For the local bumping reliability, the focus is on the ELK layers which are the critical locations affecting the package's reliability. The local finite element simulation is conducted to compare the critical ELK layers stresses with BOL structure vs. with traditional BOC structure.

Keywords: ELK, flip chip, solder bump, copper column, C6, Bonded-on-Lead

Introduction and History

Demand for cost reduction in the form of reduced die size, increased signal I/O, higher performing devices, and more system integration is pushing wafer foundries toward more advanced die node technologies, like 28Nm and beyond. More advanced die nodes require the use of extra low K (ELK) and ultra low K (ULK) dielectric layers, which are more susceptible to cracking from the stresses that naturally arise with CTE mismatch between the die and substrate.

Previously, the area of most concern with CTE mismatch was the ability of the bumps to take up this mismatch without catastrophic crack in the bump, bump to die interconnect, or bump to substrate capture pad interface [1,2]. In addition to this failure mode, there now exists an added failure mode of ELK cracking or what is commonly referred to as "white bump". Smaller die combined with higher I/O requires a higher effective signal escape/bump pitch, which in turn requires the use of a reduced bump diameter to prevent solder bridging. This causes a reduced stand off height between die and substrate, which only serves to exasperate the stress problem. The industry-wide, pb-free mandate also generates a myriad of complications since the elastic modulus and yield strength of Pb-free bumps are significantly higher than that of conventional Eutectic bumps and higher melting temperatures are required (260 deg C) to melt the pb-free alloy during die attach, which translates into higher thermally induced stresses at room or operating temperatures.

Trend of Interconnection

The use of Cu column (with Pb-free cap) as an interconnect is very appealing for bump pitches less than 150 um. Cu Columns can be plated with diameters much less than standard solderbumps and since the Cu does not collapse during reflow, the die can have a greater stand off height. One problem inherent with Cu column and pb-free solder is that the increased bump stiffness transfers more of the stress toward the die and ELK layers. Figure 1 shows a schematic drawing of the traditional flip chip solder bump and a copper column with solder cap structure on the substrate. The Young's modules of solder is in the range of 50K MPa, but the bulk copper Young's modulus is around 120MPa, which is about three times of SnAgCu solder.

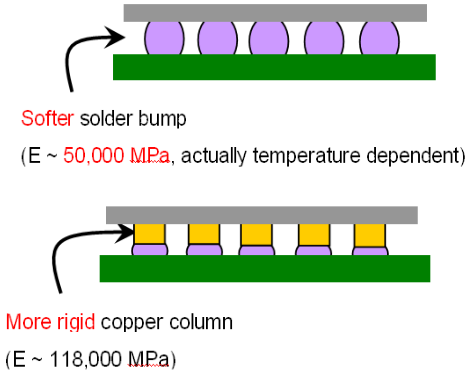

Figure 1.

Figure 2 shows actual photographs of die with ELK layer cracks which occurred during die attachment. During the process of die attachment, when the die is bonded with the substrate and they both begin to cool, the CTE mismatch between the die and substrate causes stress in the bumps. It is during the die attach process that the die is most susceptible to ELK cracking. This is because underfill has not yet been applied to help absorb the stress caused by CTE mismatch. The ELK which is closest to the UBM endure very high stresses during the solder attachment step. Larger die and higher CTE mismatch induces larger stress and creates a greater likelihood of ELK cracking.

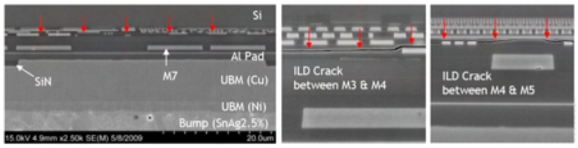

Figure 2. The ELK layers cracking during the die attachment.

Solution of the ELK layer cracking

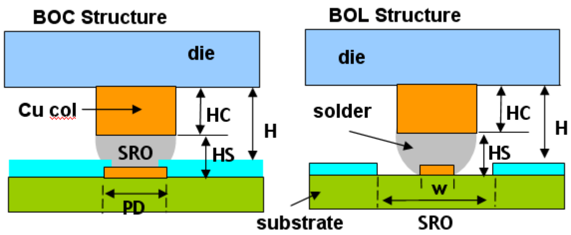

Figure 3. BOC vs. BOL structure

To avoid ELK cracking, STATS ChipPAC has proposed a unique structure to lower the stresses on the ELK layers. The basic idea is to make the interconnection more flexible and compliant when bonding the die and substrate together. Figure 3 shows the structures for the BOC vs. BOL cases. The Bond On Capture Pad (BOC) interconnect has a larger contact area with the copper pad on the substrate, which makes the package's components more rigidly bonded together and hence the structure is not flexible. The CTE mis-match between the die and substrate will cause high stresses in the ELK layers for this configuration. On the contrary, the Bond On Lead (BOL) interconnection structure has a much smaller neck area at the bottom of the solder cap. The configuration is more flexible because the structure becomes more slender. That is, the ratio of height to diameter becomes larger. Another fundamental difference between the two structures is that, the bonding mechanism of BOC is basically an interfacial attachment. The instance of interfacial cracking at the bump to solderpad interface has been well documented [3]. With the BOL structure solder also bonds to the edges of the trace which creates a more robust interconnect with no observed cases of substrate pad to bump pad interfacial failures. In summary, to reduce the ELK layers stresses, a more flexible global structure is preferred but a more rigid local bonding mechanism is better. BOL with its unique configuration meet the two requirements.

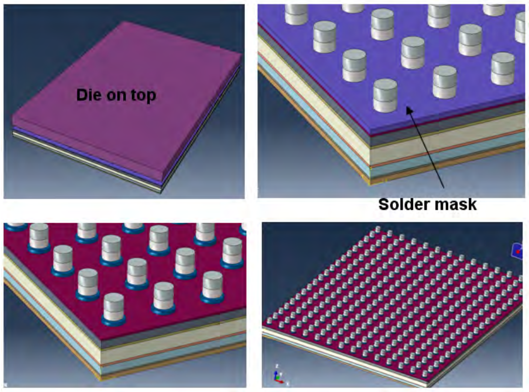

Figure 4. Global modeling of the packages

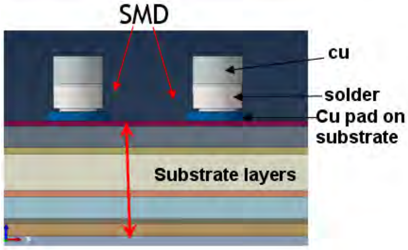

Figure 5. Modeling of the key features required for global modeling

Simulation to verify the trend

In this paper, besides the experimental data, a FEM simulation was conducted to verify that BOL is better than BOC in reducing ELK layers stresses. For the first step of the simulation, a global model is built to include the interconnections layout and the numbers of interconnections. For this regard, there are two approaches. The first one is to model the exact bumping numbers and their locations, and the second one is to assume an uniform distribution of the interconnections. For the package studied in this paper, the bumps are basically very uniformly distributed beneath die, so the second approach is used. If the bumps are not uniformly distributed and the bumping density varies a lot at different locations, then the first approach is required. While doing the global modeling, the most basic features must be included in the simulation. The features here refer to the BOC and BOL structures on each bump. Although BOC and BOL are local features, when the effects of these local structures sum up together, they will affect not only the global package's deformation, but also, in the end, affecting the stresses on the local ELK layers.

On Figure 4, the BOC is used as the example to do global modeling. The global model includes the die, copper columns, solder caps, solder mask, and detailed substrate layers. Figure 5 illustrates the solder masked defined solder bump, with the solder mask removed from the figure for clearer view, bonded on captured (BOC) pad configuration. Similarly, for the solder bump bonded on lead (BOL) configuration, the structures must be included in the global model to obtain reasonable simulation result.

Modeling of the Substrate

Modeling of all the detailed trace routing is prohibitive in terms of the computational budget and therefore it is not used here. In this paper, a micromechanics approach is used to calculate effective material properties of the substrate layers [4]. The effective material properties of Young's modulus (E), poisson ratio (ν), and CTE (α) are calculated based on the equations below, whereas *f* refers to the copper trace, *m* refers to the solder mask or substrate prepreg layers, *V* is the volume percentage.

$$E = E_f V_f + E_m V_m$$

$$\nu = \nu_f V_f + \nu_m V_m$$

$$\alpha = \frac{\alpha_f E_f V_f + \alpha_m E_m V_m}{E_f V_f + E_m V_m}$$

The formulas account for the volume percentages of the copper traces and the other component. The other components here refer to either substrate prepreg or solder mask. To calculate the volume percentage, a software tool CAM350 is used. In the current simulation, the impact from via between the layers is not considered and therefore ignored because their volume percentage is small.

Figure 5 shows the C-SAM of the test devices. The left top two figures are the packages built with BOL structure and the right top two figures are the packages built with BOC structure. C-SAM here is used to detect the delamination or cracking inside the packages. If there is a crack, the C-SAM will show the white spots on the pictures and here we refer to the white spots as the white bumps. The C-SAM was taken after the die attachment and after the filling and curing of the underfill. The figure shows that the devices built with BOC structure have lots of white bumps after the die attachment and after the filling and curing of the underfill, while the devices built with BOL structure do not have any white bumps. From the viewpoint of physics, the ELK layers will encounter the highest stresses during the die attachment process, and most of the white bumps occurred at this step, because at this step, the local ELK layers above the bumps encountered all of the forces from the CTE mis-match between die and substrate, during the die attach reflow process. The C-SAM shows that, for the package built with BOC structure, the outer row of bumps at the edge of the die have the delamination or white bumps. The bottom right of figure 5 is the finite element modeling. The package is symmetrical in X and Y direction so a quarter model is used. In order to capture the distribution of the stresses, a stress distribution along the die edge, as the red arrow line shown on the figure, is plotted. The path plot of stresses will indicate the differences between the BOC and BOL structures.

From Figure 5, the distribution of white bumps is mostly and randomly located near the four sides of the die edge, and this is obvious because of the higher stress at those locations. To study the risk of the white bumps, the finite element simulation must consider the stress distribution near the die edges. Therefore, a path plot of stresses along the die edge is analyzed to indicate the variation of the stresses, so the risk can be estimated.

Due to the complexity inherent in the metal pattern layout in the die and trace routing in the substrate, the prediction of white bump failure locations is not feasible. The path plot of stress distribution, as shown in figure 5, which is different from a deterministic approach, involves the studying of the statistical fluctuations of the maximum principle stress along the die edge. The path is chosen to pass through all the interconnections on the die edge.

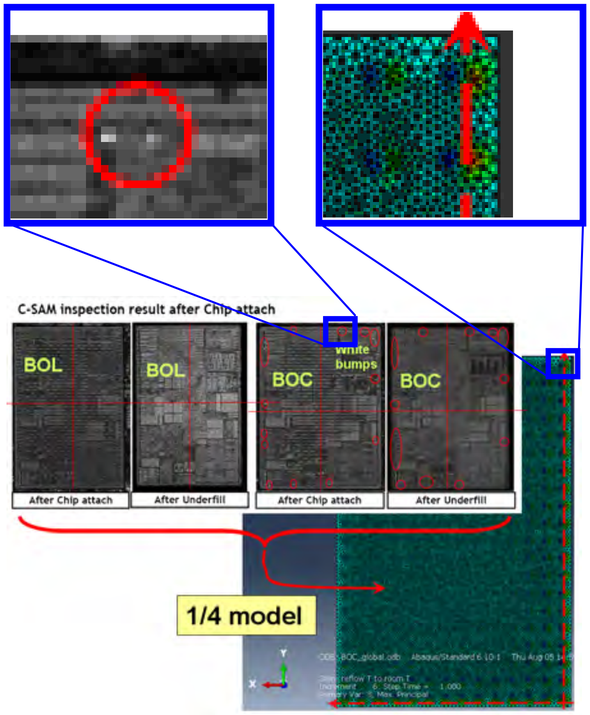

Figure 5. C-SAM of white bumps on packages built with BOL vs. BOC structures and the finite element simulation model.

The top figure on figure 6 is the path plot of maximum principal stresses for the package built with BOC structure. The peaks on the figure are the stresses in the silicon, which directly correlate to the actual Cu column with BOC interconnection. This graph shows that it is the interconnections which are undergoing the highest stresses, while in between the interconnections, the stresses drop to very low level. The averaged stress for this case is around 230 MPa. The middle figure shows the result for a BOL interconnect structure. The result shows that the BOL, with an averaged maximum principle stress of only 160MPa, has a much more compliant structure than the BOC structure and is therefore able to avoid The catastrophic white bump failures seen with the actual test parts. The bottom figure shows the stress inherent with a traditional solder bump with Pb-free solder material together with a traditional BOC structure. The data which shows averaged principle stress around 200MPa, again, shows that copper column with BOL structure is better in reducing the occurrence of white bump failure during die attach.

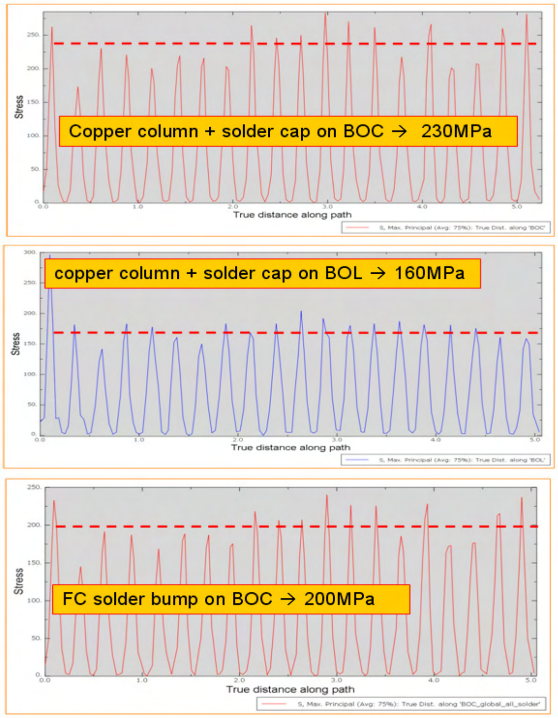

Figure 6. The maximum principle stress on the die, along the die edge path, passing through the locations where interconnections are located.

Coupling of Silicon and Substrate

During the die attachment step, because the silicon shrinks less and the substrate shrinks more, stresses are induced in the interconnections and ELK layers, which leads to white bump failure. To lower these stresses, the coupling of silicon and substrate has to be reduced. The BOL structure due to its much smaller neck area at the base of the interconnections, can reduce the coupling between silicon and substrate, and figure 7 shows the benefit of the coupling. The top figure shows that, for copper column with BOL structure, the quarter model package's displacement in Z direction is -0.1010 mm, for copper column with BOC structure, the Z displacement is -0.1045, and for flip solder bumps on BOC structure, the Z displacement is -0.1039. The result shows that the Cu Column with BOL is the best in reducing the coupling which leads to package deformation.

Local Modeling of the Stresses of ELK layers

A very typical modeling of the stresses of ELK layers is to use sub-modeling techniques, and top two figures in figure 8 illustrate this method. Firstly a global model is constructed to simulate the stress, strain, and deformation behaviors of the entire model or global model. The model usually does not include detailed features, such as UBM and ELK layers, because the scale or dimension of UBM and ELK layers are about 2 to 3 orders of magnitude smaller than the package's dimensions. The approach is actually more practical because accounting for all detailed features in the global model is very time consuming and memory demanding from the viewpoint of the computation, especially when the budget is a concern. After the global modeling, a small portion of the global is cut out and revised to include the desired features such as UBM and ELK layers. The bottom two figures, on figure 8, show that the detailed features of UBM, ELK layers, BOC, and BOL are all included in the local modeling. Figure 9 illustrates the maximum principle stress of the critical ELK layer and the result shows that the BOL structure causes lower stress.

As mentioned previously, due to the complexity inherent in the metal pattern layout in the die and trace routing in the substrate, it is not surprising to see that actual locations of white bump failures in the test parts appears to be random. In order to get a more representative stresses of ELK layers, more local models at different locations is suggested. The locations of local models can be picked either manually or by a numerical looping to adjust the locations automatically. Figure 9 shows one example of the local model. When computer resource is not a concern, a model which includes all the detailed features is preferred and the work is currently under development by the authors using distributed parallel simulation.

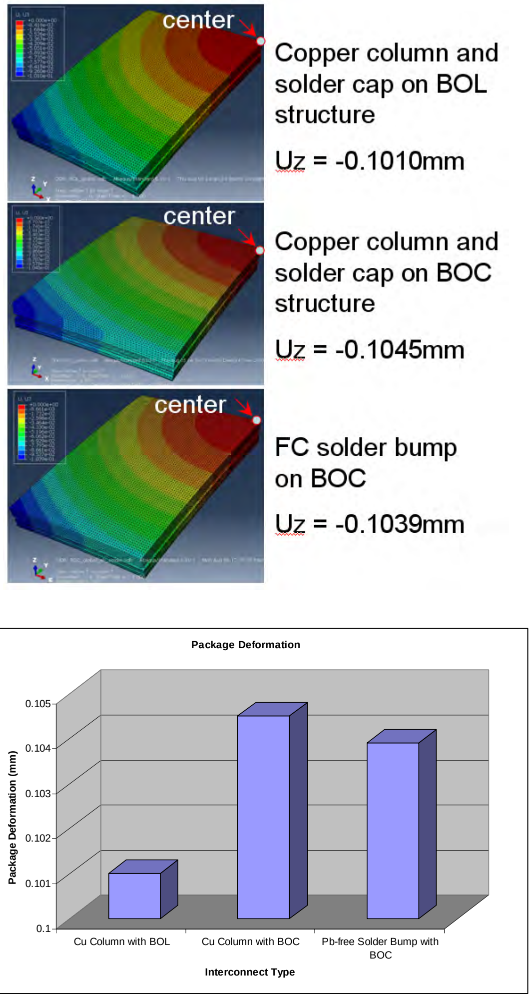

Figure 7. Deformations of the packages

Conclusions

In summary, the paper demonstrates that the packages built with Bond on Lead (BOL) structure is superior to traditional packages built with Bond on Captured (BOC) pad structure. Simulation data is able to prove that the trend of the stresses of silicon and ELK layers match with the experimental data. The STATS ChipPAC's BOL technology provides an excellent solution to achieve reliable packages without the issues of ELK layer damage.

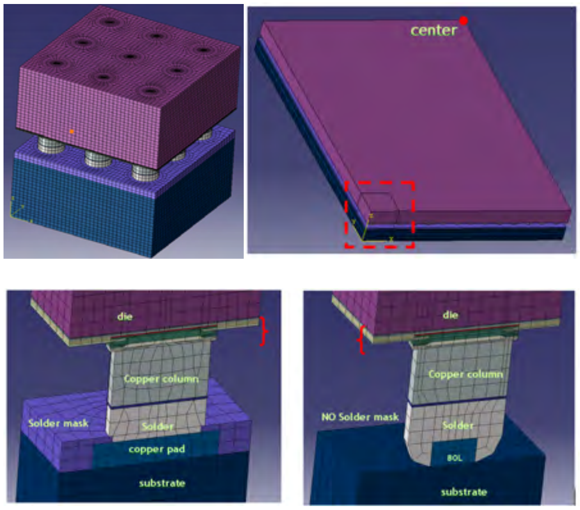

Figure 8. Global and local modelings

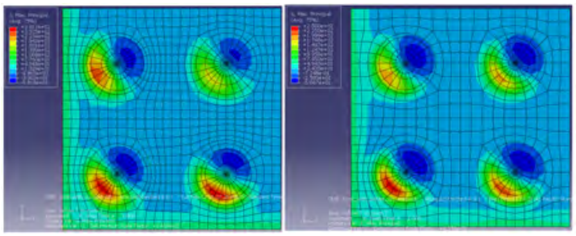

Figure 9. Global and local modelings

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