

Advanced Semiconductor Assembly and Test

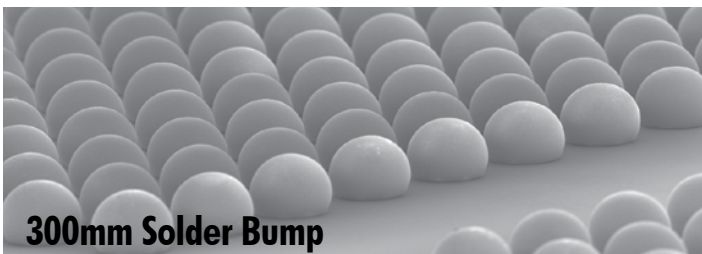
Wafer Level Processing

As one of the fastest growing package types in the semiconductor industry, Wafer Level Packages (WLP) offer a small, lightweight, high performance device that is a cost effective solution for mobile and consumer applications. With state-of-the-art 300mm manufacturing capabilities and advanced process technologies such as low cure temperature polymers, under bump metallization (UBM) and redistribution layers (RDL), STATS ChipPAC Taiwan is a leader in wafer bump and WLP solutions.

Wafer level packages differ from laminate and leadframe based packages in that all of the manufacturing process steps are performed in parallel at the silicon wafer level rather than sequentially on individual semiconductor chips. A Wafer Level Chip Scale Package (WLCSP) is essentially the same size as the die, providing a high performance package in a more compact package footprint than conventional manufacturing processes. At STATS ChipPAC Taiwan, WLCSPs are manufactured with advanced process technologies such as electroplated copper RDL and UBM to achieve higher densities and increased reliability for customers.

Wafer Bumping Services

Wafer bumping is a process in which interconnections (solder “bumps” or “balls”) are formed on an entire wafer prior to dicing. The use of wafer bumping is driven either by the need for high performance, high I/O densities, small form factor or array interconnect requirements.



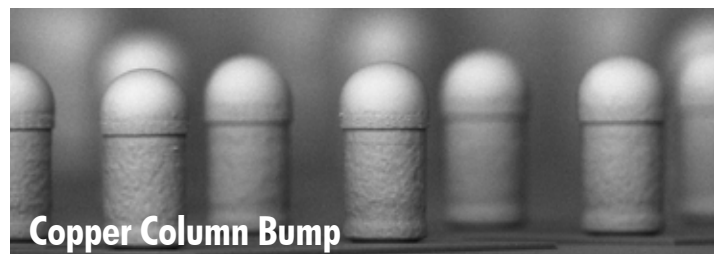
300mm Solder Bump

STATS ChipPAC Taiwan’s world-class solder bumping line offers high volume production capability for 300mm wafers. This state-of-the-art facility provides eutectic and solder alloy (low alpha) and leadfree soldering bumping.

Technology	Plating bump (300mm)
Bump material	Eutectic & Pb Free (Ultra Low Alpha)
Solder material	Sn63/Pb37 (Eutectic)
	Sn98.2/Ag1.8 (Pb Free)
UBM Structure	Sputter Ti/Cu and Plating Cu/Ni
Minimum bump pitch	150 μ m
Bump height & size	80 μ m / 100 μ m
Wafer Probe Test	Available

Wafer Level Capability and Process Flow

	PROCESS FLOW	MATERIAL	
Bumping	Direct Bump (FOC)		
	Wafer Incoming		
	UBM Pattern	Ti/Cu/Ni, Ti/Cu/Cu/Ni	
	Bump Forming	Eu/LF bump	
	Final Inspection		
	Shipping		
	Repassivation (REPSV)		
	Wafer Incoming		
	PI Pattern	PI	
	UBM Pattern	Ti/Cu/Ni, Ti/Cu/Cu/Ni	
	BUMP Forming	Eu/LF bump	
	Final Inspection		
	Shipping		
	Redistribution (RDL)		
	Wafer incoming		
Post Bump Sort	PI1 Pattern	PI/PBO	
	RDL Pattern	Ti/Cu/Cu	
	PI2 Pattern	PI/PBO	
	Bump Forming	Ball Drop (SAC105/SAC405)	
	Final Inspection		
	Shipping		
	Backend Process	Wafer incoming	
		Wafer Backside Laminate (option)	
		Backside Laminate (option)	
		Laser Mark	
		Wafer Mount	
		Wafer Saw	
		Wafer Laser Grooving (option)	
		Tape and Reel	
		Shipping	



Copper Column Bump

Copper column bump provides a high performance, cost effective solution for advanced silicon fab nodes. STATS ChipPAC Taiwan is experienced in copper column bump technology which enables a higher I/O density in very fine bump pitches down to 80 μ m with a higher resistance to electromigration.

Technology	Copper column bump (300mm)
Bump material	Copper column
Solder material	Cu ₂ Ni/Pb free Solder (1.8%Ag)
UBM Structure	Sputter Ti/Cu
Minimum bump pitch	80 μ m
Bump height & size	<=80 μ m / >=40 μ m

Your Wafer and IC Testing Partner in Taiwan

Finding the right test solution to meet your needs is essential in today's competitive market. As one of the leading test houses in Taiwan, STATS ChipPAC Taiwan offers proven expertise in mixed-signal, digital, embedded memory, consumer optics and wireless applications.

With strategic relationships in place with the major foundries and assembly houses, STATS ChipPAC Taiwan can provide full turnkey test and assembly services for a smooth, uninterrupted delivery of your product. Our portfolio of advanced test platforms, experienced R&D and engineering teams can reduce your engineering burden and ready your product for commercial success in the shortest time possible.

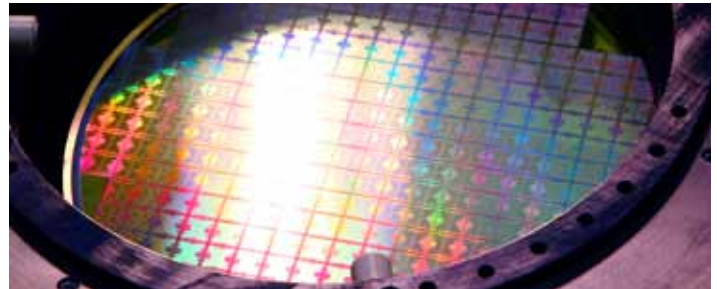
Quality and time-to-market are two of the critical factors in the success of your product. To ensure you receive the highest level of quality, STATS ChipPAC Taiwan has achieved top industry certifications including ISO9001, ISO14001, TS16949 and OHSAS18001.

STATS ChipPAC Taiwan's experience and focus on wafer bump, wafer sort, CMOS Image Sensors and final test will ensure that you receive the right test solution for your business requirements.

Turnkey Test Services

STATS ChipPAC Taiwan offers a full spectrum of turnkey services including:

- Incoming inspection
- Wafer probe / bumped wafer probe
 - 300mm wafer probe / bumped wafer probe
 - Vertical wafer / bumped wafer probe
 - Laser trim
- Final test
- Dry-bake, packing, tape and reel
- Drop shipment to your end customer



Test Platforms

Manufacturer	Model	System Capability
Advantest	T2000	Mixed-Signal
Credence	SC312	50 MHz Logic
Teradyne	I-Flex	Mixed-Signal
Teradyne	I-Flex RF	RF & Mixed-Signal
Teradyne	UltraFlex	Mixed-Signal
Teradyne	Catalyst	Mixed-Signal
Teradyne	J750	100 MHz Logic
Verigy	93000	Mixed-Signal
Verigy	94000	Mixed-Signal
Verigy	PS800	Mixed-Signal
Verigy	PS400	Mixed-Signal
Verigy	PS400	RF & Mixed-Signal



STATS ChipPAC Taiwan
 No. 176-5, 6 Ling, Lu Liao Ken, Hua Lung Chun, Chiung Lin
 Hsin-Chiu Hsien, Taiwan, R.O.C. 307
 Tel: 886-3-593-6565 / Fax: 886-3-593-6363
www.statschippac.com.tw